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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,282	11/20/2003	Koji Tanonaka	FUJI 20.756	3194

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EXAMINER	
NAJEE-ULLAH, TARIQ S	
ART UNIT	PAPER NUMBER
2152	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/719,282	TANONAKA, KOJI	
	Examiner	Art Unit	
	TARIQ S. NAJEE-ULLAH	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/20/03, 12/12/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

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DETAILED ACTION

This is the first Office action in response to Application 10/719,282 filed on 20 November 2003. Claims 1-9 have been examined and are pending.

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 20 November 2003 and 12 December 2007 were in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the

prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipate by US Patent 6,618,455 to Maeda et al (Maeda hereinafter).

Regarding claims 1 and 4, Maeda teaches **a synchronous network establishing method of establishing a synchronous network in which a node apparatus conforming to a first scheme and a node apparatus conforming to a second scheme co-reside** (col. 1, line 60 – col. 2, line 16)**; converting a first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme** (clock signal, col. 2, lines 5-35) **and the second scheme into a second synchronization state indication code for the node apparatus conforming to the other one of the first scheme and the second scheme** (clock signal, col. 2, lines 5-35)**.**

Regarding claim 2, Maeda teaches the invention substantially as described in claim 1 above including, **further comprising the step of: including the first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme and the second scheme in an empty bit** (fig. 2, col. 5, line 37-56) **of the converted second synchronous state indication code** (clock signal, col. 2, lines 5-35)**.**

Regarding claim 3, Maeda teaches the invention substantially as described in claim 1 above including, **further comprising the step of: using a pre-converted synchronous state indication code included in an empty bit** (fig. 2, col. 5, line 37-56) **of the first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme and the second scheme** (clock signal, col. 2, lines 5-35)**.**

Regarding claim 5, Maeda teaches the invention substantially as described in claim 4 above including, **further comprising: a selecting unit for selecting one of the synchronous state indication code supplied from the counterpart node** (fig. 16, col. 4, line 27-61) **and the converted synchronous state indication code obtained by the synchronous state indication code converting unit** (clock signal, col. 2, lines 5-35)**.**

Regarding claim 6, Maeda teaches the invention substantially as described in claim 5 above including, **wherein the selecting unit administers switching according to a switching instruction signal** (clock switching unit, col. 1, line 66 – col. 2, line 35)**.**

Regarding claim 7, Maeda teaches the invention substantially as described in claim 5 above including, **further comprising: a switch unit**

for instructing a switching of the selecting unit (clock switching unit, col. 1, line 66 – col. 2, line 35)**.**

Regarding claim 8, Maeda teaches the invention substantially as described in claim 5 above including, **further comprising: a switching instruction unit for detecting a predetermined bit of a signal supplied from the counterpart node apparatus to determine which of the first scheme and the second scheme said counterpart node apparatus conforms to, and instructing a switching of the selecting unit based on the determination** (clock switching unit, col. 1, line 66 – col. 2, line 61)**.**

Regarding claim 9, Maeda teaches the invention substantially as described in claim 4 above including, **wherein a content to be converted by the synchronous state indication code converting unit can be arbitrarily changed** (clock switching unit, col. 1, line 66 – col. 2, line 61)**.**

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent 6,006,069 to Langston.
- US Patent 6,118,795 to Fukunaga et al.
- US Patent Application Publication 2001/0017866 to Takada et al.
- US Patent Application Publication 2002/0006110 to Brezzo et al.

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- US Patent Application Publication 2002/0041602 to Kageyama et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TARIQ S. NAJEE-ULLAH whose telephone number is (571)270-5013. The examiner can normally be reached on Monday through Friday 8:30 - 6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on (571) 272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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T. N.

/Jeffrey Pwu/
Supervisory Patent Examiner, Art Unit 2146